CLAIMS

1. A circuit arrangement for deriving phase conjugation information from a main input signal of a given frequency comprising:

an input receiving a reference input signal; and

a phase locked loop (PLL) circuit comprising an oscillator having a main output signal, an input receiving a PLL input signal, an input receiving a feedback signal from the oscillator and a phase detecting means,

wherein the phase detection means detects any phase difference between the PLL input signal and the feedback signal and provides a phase control signal to the oscillator.

2. A circuit as claimed in claim 1, wherein a first heterodyne mixer mixes the main input signal and the main output signal to provide the feedback signal and the PLL input signal is the reference input signal.

3. A circuit as claimed in claim 2, wherein the feedback signal is the up-converted mixing product of the first heterodyne mixer.

4. A circuit as claimed in claim 3, wherein the frequency of the reference input signal is scaled to match the frequency of the feedback signal.

5. A circuit as claimed in any preceding claim, wherein the feedback signal is scaled.

6. A circuit as claimed in any preceding claim, wherein the phase detection means is a digital phase detector.

7. A circuit as claimed in any of claims 1 to 5, wherein the phase detection means also detects any phase difference between an input receiving the main output signal and an input receiving the reference signal thereby creating a further phase locked loop.

8. A circuit as claimed in claim 7, wherein the phase detection means comprises:

a first phase detector which detects any phase difference between an input receiving the reference input signal and an input receiving the feedback signal;

a second phase detector which detects any phase difference between an input receiving the reference input signal and an input receiving the main output signal;

an integrator integrating the first phase detector output;

an oscillator heterodyne mixer for mixing the integrator output and the second phase detector output;

wherein the oscillator mixer output is the phase detection means output providing a control signal for the oscillator.

9. A circuit as claimed in any of claims 1 to 5, wherein the phase detection means comprises:

a first phase detection heterodyne mixer mixing an input receiving the reference input signal and an input receiving the feedback signal and having a first phase detection mixer output wherein the first mixer output is the down-converted mixing product of the first mixer;

a second phase detection heterodyne mixer mixing an input receiving the reference input signal and an input receiving the first phase detection mixer output and having a second phase detection mixer output wherein the second phase detection mixer output is the down-converted mixing product of the second phase detection mixer and the phase detection means output providing a control signal for the oscillator.

10. A circuit as claimed in claim 1, wherein a feedback heterodyne mixer mixes an input receiving the main output signal and an input receiving the reference input signal, the feedback signal is the down-converted mixing product of the feedback heterodyne mixer and the PLL input signal is the main input signal, the feedback signal being proportional to the main input signal.

11. A circuit as claimed in claim 10, wherein the main input signal is scaled by a first divider,

the main output signal is scaled by a second divider and the feedback signal scaled by a third divider, the first divider having a scaling value equal to the product of the second and third divider scaling values.

12. A circuit as claimed in claim 1, wherein an input heterodyne mixer mixes the main input signal and the reference input signal, the PLL input signal is the down-converted mixing product of the input heterodyne mixer and the feedback signal is the main output signal, the main input signal and the main output signal having substantially equal frequencies.

13. A circuit as claimed in claim 12, wherein a first divider scales the main input signal, a second divider scales the main output signal, the first divider having a scaling value equal to the second divider scaling value.

14. A circuit as claimed in any preceding claim, wherein the oscillator is a voltage controlled oscillator (VCO).

15. A method of deriving phase conjugation information from an input signal, the method comprising detecting phase difference in a phase locked loop (PLL) circuit between a feedback signal having a first frequency and a PLL input signal of a second frequency which is proportional to the first frequency.